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MOSFET as a Switch

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Abstract

MOSFETs can be used as a switch in mixed signal design for many purposes. This paper describes the working of MOSFETs as a switch. Also it shows the different problems and some remedy to solve those problems with equations and simulations.

Keywords: Dual Vth, Transistor Stack, Sleep Transistor, Forced Transistor Stack, MTCMOS, VTCMOS, SCCMOS, , LECTOR, GALEOR

Introduction

Compared to BJT a MOS transistor is more preferable as a switch because (a) it can be on while carrying zero current, and (b) its source and drain voltages are not "pinned" to the gate voltage i.e. if the gate voltage varies, the source or drain voltage need not follow the variation. Figure shows the symbol for n-type MOSFET, revealing three terminals: Gate (G), Source (S) and Drain (D).

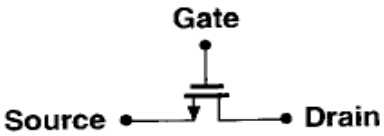

Fig.1 Simple view of a MOS device[1]

When Operating as a switch, the transistor connects the source and drain terminals together if the gate voltage V_G is high and isolates the source and drain ifV_G is low. The source and drain terminals are interchangeable because the device is symmetric i.e. a MOS can conduct current in either direction by simply exchanging its source and drain terminals.

While working as a switch a MOS device is affected by various problems like channel charge injection, clock feed through. Also in "ON" condition a MOS device has some finite resistance known as on-resistance significantly affect the performance during operation.

MOSFET as a Switch

As shown in figure 2 a MOS can be directly used as a switch.

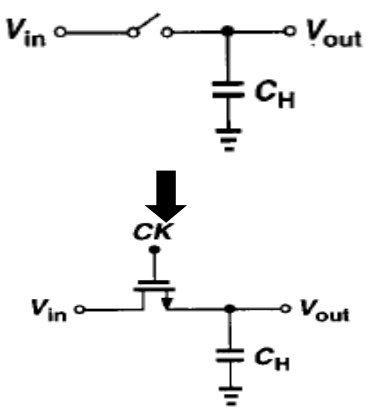

Fig.2 Implementation of a switch by MOS device[1]

When gate command CK goes high MOS switch works as a controlled linear resistor and when clock command goes low MOS work as open circuit as shown in figure 3.

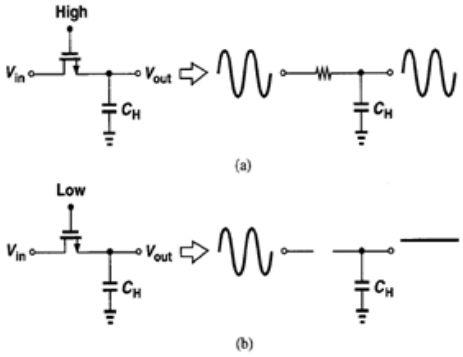

Fig.3 (a) CK command HIGH, (b) CK command goes LOW [1]

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Operation Regions

Cut-off Region : *(* V_{GS}<V_{TH}*)*

When gate to source voltage (V_{GS}) is less then threshold voltage(V_{TH}) the MOS device is in cutoff region. There is no current flow from drain to source in device.

Linear or Triode region: $(V_{DS} \leq V_{GS} - V_{TH})$

As increase in gate to source voltage, drain to source voltage also increases. When V_{GS} is greater then V_{TH} MOS device enters in linear region where drain current linearly increases with increase in V_{DS} and is given by,

$$I_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2} {V_{DS}}^2] \quad \text{.... (1)}$$

When V_{DS}=$(V_{GS} - V_{TH})$, the drain current is maximum and given by,

$$I_{D,\,max} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad \text{.... (2)}$$

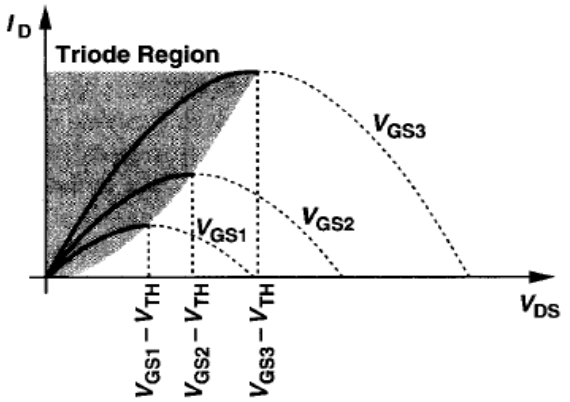


Fig.4 Drain current versus drain source voltage in triode region [1]

Further increase inV_{DS}, MOS device operates in saturation region.

Saturation region: V_{DS}>$(V_{GS} - V_{TH})$

When V_{DS}>$(V_{GS} - V_{TH})$, the drain current does not followV_{DS}. Instead it,$I_D$becomes relatively constant and device operatesin saturation region.

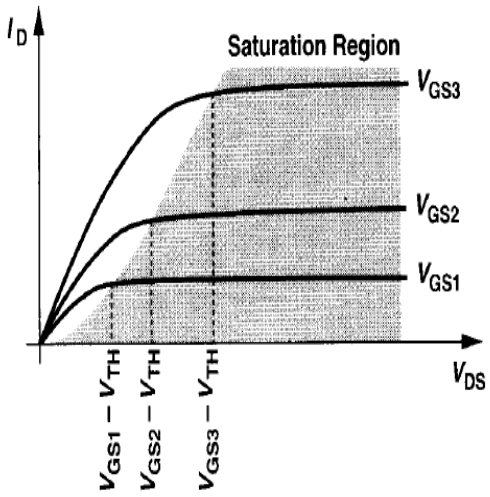
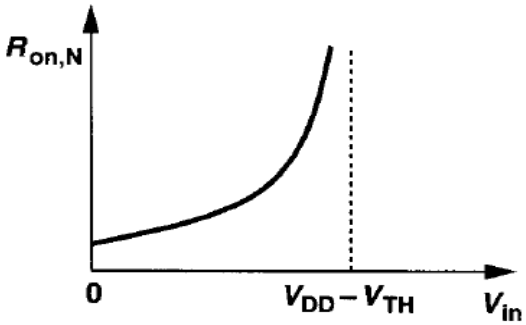


Fig.5 Drain current in saturation region[1]

Switch On-Resistance

To turn an NMOS switch on, the clock signal on its gate goes up to the supplyvoltage (V_{DD}), and the resultant $(V_{GS} - V_{THN})$ becomes larger than V_{DS}. Thus, thetransistoris working in the triode region and the relationship between$I_D$and V_{DS} can beexpressed by Equation (1). Ignoring the body effect, we can derive the transistor'sequivalent drain-source resistance (i.e., the switch on-resistance) by dividing V_{DS} byld, and we have

$$R_{ON} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{THN})} \quad \text{.... (3)}$$



(a)

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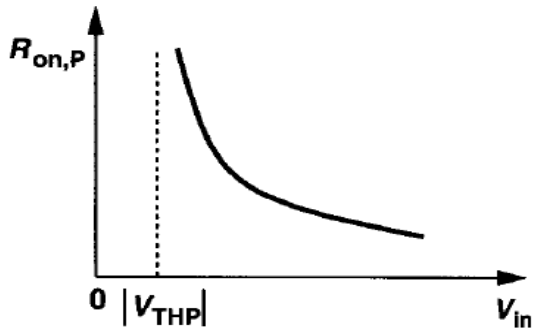
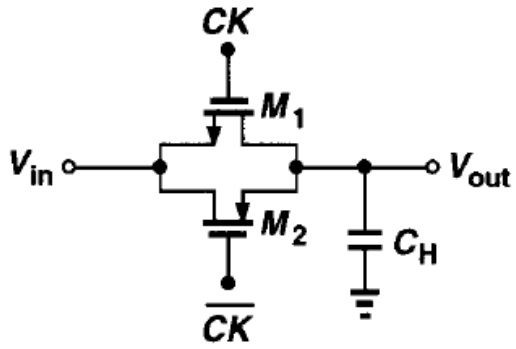


(b)

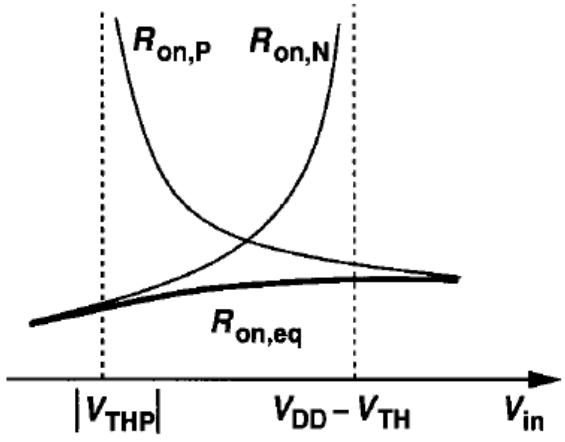
Fig.6 On Resistance of (a) nMOS(b) pMOSdevices[1]

For a typical PMOS transistor, the value of $\mu_p C_{ox}$ is very small compared to $\mu_n C_{ox}$ for its NMOS counterpart; therefore thePMOS transistor is less attractive when it comes to realizing a switch of low on-resistance.

The CMOS transmission gate is a better candidate than both NMOS and PMOS transistors in terms of reducing the on-resistance.



(a)



(b)

Fig.7 (a) Complementary switch (b) on resistance of the complementary switch [1]

Non-linear Effects of MOSFET Switches

A. Channel Charge Injection Effect

When MOS device is on (Fig. 2), a channel exists at oxide channel interface. Total charge in the inversion layer,

$$Q_{ch} = WLC_{ox}(V_{dd} - V_{in} - V_{th}) \quad \ldots. (4)$$

When switch turns off Q_{ch}exists through drain and source terminals. This is known as channel charge injection.

Total charge divided between the source and drain depends on (a) clock turnoff slope, (b) the ratio of the input capacitance to output capacitance (C_{in}/C_{out}), (c) the drain-source voltage

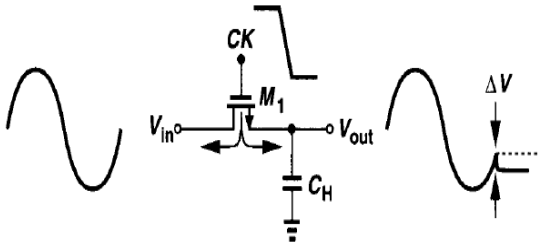


Fig.8 Effect of channel charge injection [1]

Effect of channel Charge injection can be solved by,

(1) Using dummy switch

Fig. (9) Shows an alternative charge injection compensation configuration here adummy switch is added next to the main switch. As shown in Fig. (9), the sizeof the dummy switch is set as one-half that of the main switch, and the dummy'sdrain and source are shorted. When the mainswitch is turned off, half of the channel charge flows through the dummy switchtoward the hold capacitor (Cs).

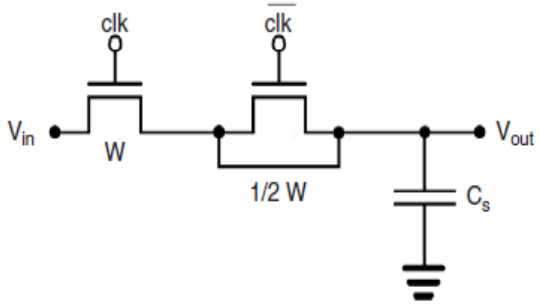


Fig.9 Use of dummy switch to compensate charge injection [1]

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(2)Using Complementary Switch

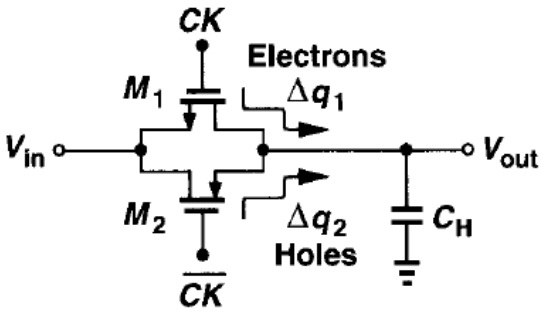

Fig.10 Use of Complementary Switch to reduce the effect of channel charge injection[1]

In complementary switch, opposite charge packets injected by two channels cancel each other.

B. Clock feedthrough Effect

Clock feedthrough can be understood with the help of Fig.11. The capacitances between the gate/drain and gate/source of the MOSFET are modelled with the assumption that the MOSFET is operating in the triode region. When the gate clock signal goes high, the clock signal feeds through the gate/drain and gate/source capacitances.

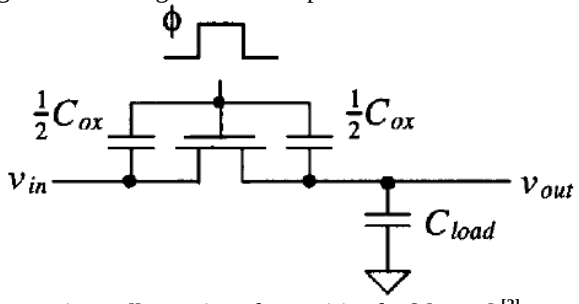

Fig.11 Illustration of capacitive feedthrough[2]

Now, as the switch turns on, the input signal, V_{in} is connected to the load capacitor through the NMOS switch. The result is that C_{load} is charged to V_{in} and the capacitive feedthrough has no effect on the final value of V_{out}. When the clock signal makes the transition low, that is, the n-channel MOSFET turns off. A capacitive voltage divider exists between the gate-drain/gate-source capacitance and the load capacitance. As a result, a portion of the clock signal appears across C_{load} as

$$\Delta v_{load} = \frac{C_{overlap}\ (V_{DD} - V_{ss})}{C_{overlap} + C_{load}} \quad \ldots. (5)$$

Where $C_{overlap}$ is the overlap capacitance.

$$C_{overlap} = C_{ox}\, W.LD \quad \ldots. (6)$$

Where LD is the gate length of the gate that overlaps the drain/source.

Effect of clock feedthrough can be solved by,

(1) Using Dummy Switch

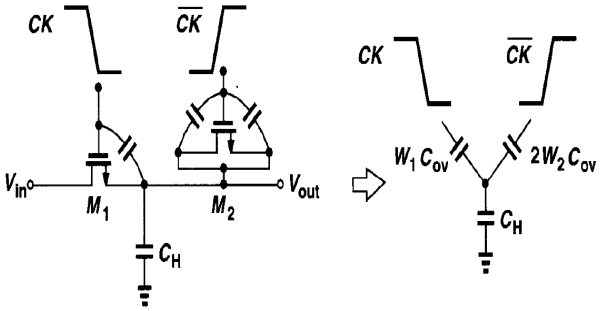

Fig.12 Clock feedthrough suppression by dummy switch [1]

Shown in the fig.12 the effect of clock feedthrough is suppressed through dummy switch. The total charge in V_{out} is zero because

$$V_{CK}\frac{W_1 C_{ov}}{W_1 C_{ov} + C_H + 2W_2 C_{ov}} + V_{CK}\frac{2W_2 C_{ov}}{W_1 C_{ov} + C_H + 2W_2 C_{ov}} = 0 \quad \ldots. (7)$$

Simulation Results in 90nm Technology

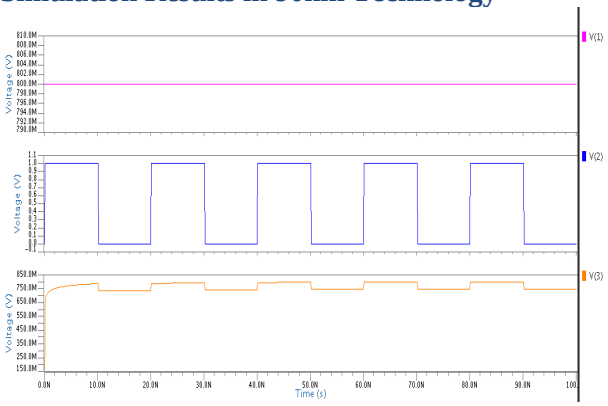

Fig.13 Effect of charge injection (DC input)

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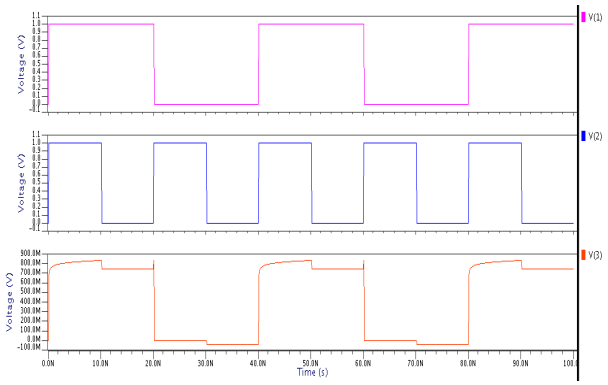

Fig.14Effect of charge injection (PULSE input)

Use of dummy switch to remove the effect of charge injection shown in the figures

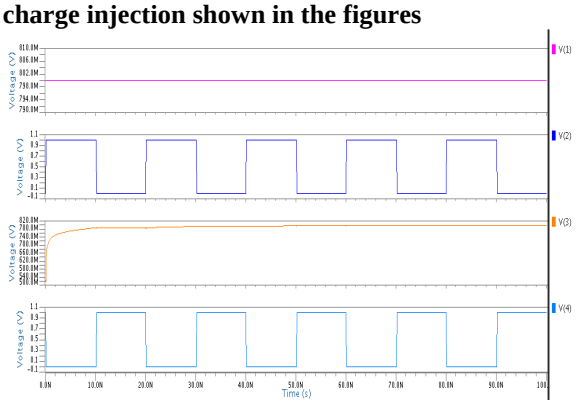

Fig. 15 Remove the effect of charge injection (DC input)

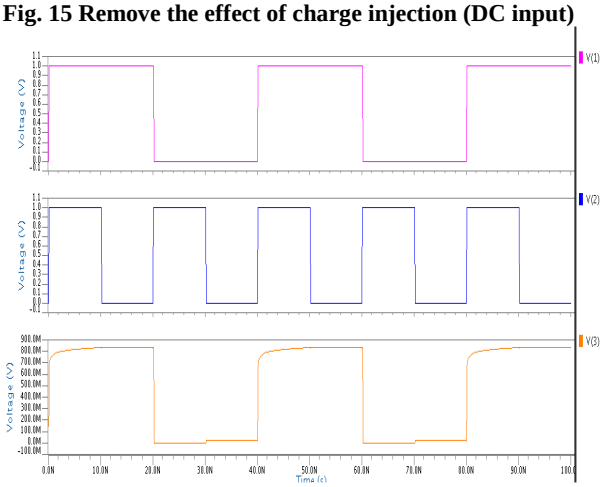

Fig.16 Remove the effect of charge injection (PULSE input)

Charge injection can be removed by using complementary switch as shown below:

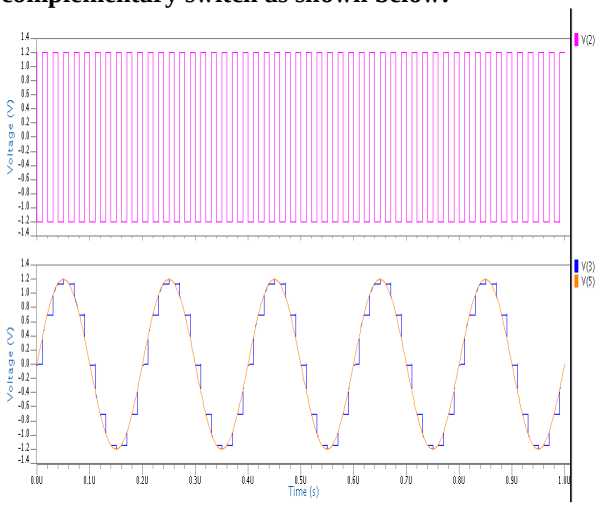

Fig. 17 Remove the effect of charge injection using complementary switch (AC input)

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